REMARKS/ARGUMENTS

Claims 2-21 are pending.

Claims 2-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,356,978, Kobayashi et al.

The present invention as recited in independent claims 2, 6, 12, and 16 include a processor and a local memory and a cache memory. The local memory and the cache memory are associated with the processor.

The Examiner cited processors (13a, 13b, Fig. 1) in Kobayashi et al. and cache memories (20a, 20b) for allegedly showing this aspect of the invention. Fig. 1 shows a module (17a) having a processor (13a) and a cache memory (20a). The figure shows a second module (17b), also having a processor (13b) and a cache memory (20b). The two modules are coupled to a system bus (18). As understood, the Examiner seems to assert that the "local memory and cache memory" recited in the pending claims somehow reads on the cache memories (20a, 20b) of Kobayashi et al. Thus, based on the Examiner's interpretation of Kobayashi et al., cache memory (20a)constitutes the "local memory" for processor (13a), and cache memory (20b) constitutes the "cache memory" for processor (13a). It is respectfully submitted that the Examiner's interpretation of local memory and cache memory are inconsistent with convention definitions. Kobayashi et al. therefore do not show this aspect of the present invention.

The foregoing distinction notwithstanding, and in the interest of moving the prosecution of the instant application to a successful conclusion, claims 2, 6, 12, and 16 have been amended to further distinguish Kobayashi et al. As amended, the claims further recite that the local memory and the cache memory contain only information that is used only by the processor. For example, claim 2 recites:

> "the local memory and the cache memory storing management information that is used only by the at least one microprocessor,
>
> the local memory and the cache memory exclusive of management information that is used by any microprocessor other than the at least one microprocessor"

Kobayashi et al. clearly do not show this aspect of the invention. In fact, they explicitly disclose that the contents of the common memories (12a, 12b) are copied to each other:

> "In operation, each of the resource management modules 17a, 17b updates the management information stored in its own common memory 12 ... and simultaneously also updates the management information of the common memory provided in the other resource management module. In this manner, the common memory 12 in each of the resource management modules 17a, 17b have the same contents." *Col. 4, lines 41-49.*

Regardless of how the cache memories of Kobayashi et al. are construed, they show that both memories contain the same information for both processors. This is teaching of Kobayashi et al. clearly is different from the present invention as recited in the pending claims, where the recited local and cache memories store information used only by the processor and is exclusive of information that is used by any other processor. For at least this reason, the present invention as recited in the pending claims is therefore believed to be patentably distinct from Kobayashi et al.

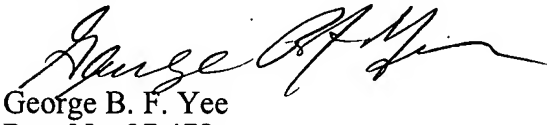
In addition, claims 2 and 6 further recite that the access speed of the local memory is higher than that access speed of the cache memory. For example, claim 2 recites "an access time between the microprocessor and the local memory to perform an access operation being lower than an access time between the microprocessor and the cache memory for the same access operation." A review of the Office action details does not indicate that this is shown in Kobayashi et al., and so for at least this reason claims 2 and 6 are believed to be allowable over Kobayashi et al.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



George B. F. Yee
Reg. No. 37,478

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
GBFY:cmm
60312982 v1